Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JANUSZ RAJSKI and JERZY TYSZER

Appeal No. 2001-2425
Application No. 09/276,474

ON BRIEF

Before KRASS, JERRY SMITH and SAADAT, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 8-28 and 35-51.

The invention pertains to testing logic functions within an integrated circuit. In particular, the logic functions are embedded so that they are not accessible by normal I/O pins of the integrated circuit. The same data paths which are used for processing

data in a normal mode of operation are also employed, via logic, in a test mode to emulate a plurality of linear feedback shift register (LFSR)-based segments to generate test patterns for peripheral devices having associated parallel scan registers coupled to the processor core of the integrated circuit.

Representative independent claim 8 is reproduced as follows:

8. An integrated circuit comprising:

a processor core including data paths for processing data in a normal mode of operation;

a plurality of peripheral devices having associated parallel scan registers coupled to the processor core; and

operating logic to operate the data paths of the processor core in a test mode of operation to emulate a plurality of linear feedback shift register (LFSR) - based segments interconnected by a network of linear functions to generate deterministic test patterns for the peripheral devices.

The examiner relies on the following reference:

Bullinger et al. (Bullinger) 4,947,395 Aug. 07, 1990

Claims 8-28 and 35-51 stand rejected under 35 U.S.C. § 103 as unpatentable over Bullinger.

Reference is made to the briefs, paper no. 5, [non-final rejection] and the answer for the respective positions of appellants and the examiner.

OPINION

It is the examiner's position that Bullinger shows a "core processor (column 4, lines 32 et seq.), a plurality of peripheral devices (16), associated scan registers (40-1, 40-n), operating logic for generating test patterns emulating a LFSR (18), interconnected by a linear network (10), and compacting responses (fig. 4)" [Paper No. 5-page 3].

While the examiner notes that Bullinger does not explicitly state that the core processor is coupled in parallel to the scan circuits, the examiner notes that Bullinger teaches that the processor is connected to parallel data bus 14 and parallel address bus 12, citing columns 3-4, and that Bullinger's testing apparatus provides one or more controlled interfaces, which are referred to as scan paths, between the data bus and the controlled interfaces, citing column 4, line 1 et seq. and column 5, line 35 et seq. [see Paper No. 5-page 3].

The examiner takes "official notice of both the concept and benefits, that it is notoriously well known in the data processing art to have a processor connected in parallel to parallel scan registers" [Paper No. 5-page 3].

From this, the examiner concludes that the artisan would have "readily realized that modifying the connections of a processor to multiple scan paths via a parallel

connection, would enable faster loading of the scan patterns and thus, faster testing of the devices" [Paper No. 5-page 3]. The examiner also contends that the artisan would have been led to make such a modification because Bullinger suggests "that scan paths such a parallel connection is useful [sic] for testing integrated logic that is connected to parallel buses (col. 4, lines 8 et seq.)" [Paper No. 5-page 3].

Bullinger clearly is a very relevant reference to the claims at hand, disclosing, as it does, access for testing embedded logic functions within an integrated circuit without requiring additional I/O pins.

The distinction argued by appellants, however, is that while, in the instant claims, normally available data paths of a processor core are operated in a test mode to implement scan testing, Bullinger uses "special-purpose" circuitry to implement a scan test [brief-page 7, reply brief-page 3]. Moreover, argue appellants, the LSFR disclosed by Bullinger is directed to output data compression and has nothing whatsoever to do with test pattern generation (reply brief-page 3). But, even assuming the LSFR is implemented using data paths of an on-chip processor core in Bullinger, appellants argue that Bullinger still does not suggest the claimed "data paths for processing data in a normal mode of operation" that are operated "in a test mode of operation...to generate deterministic test patterns," as set forth in claim 8 (reply brief-pages 3-4).

Appellants stress that this is made clear by the fact that the language of claim 8 requires the data paths of the processor core to operate "to emulate" LFSRs, so that while the data paths may not necessarily operate as LFSRs when processing data in a normal mode of operation, these data paths are used to "emulate" LFSRs in a test mode of operation (reply brief-page 4). Appellants contrast this with Bullinger's special-purpose circuitry which denote an LFSR, according to the examiner. Therefore, conclude appellants, if the circuitry is in fact an LFSR, there would be no need "to emulate" an LFSR (reply brief-page 4).

We do not agree with appellants' conclusion that if Bullinger's special-purpose circuitry is, in fact, an LFSR, then it cannot be said "to emulate" an LFSR. If an element is, in fact, itself, then it clearly "emulates" itself, as an element acting as itself is the epitome of emulation.

However, we do agree with appellants that the instant claims require the processor core to include data paths for processing data in a normal mode of operation and those same data paths are then operated, by logic, in a test mode of operation, to emulate a plurality of LFSR-based segments...to generate deterministic test patterns for peripheral devices.

While Bullinger does provide a scan testing which does not require additional pin connections, Bullinger is very clear that this is provided by the use of "additional

registers, multiplexers, and decoders in conjunction with existing buses to provide test access" [abstract]. Accordingly, Bullinger is not employing the *same* elements, or data paths, to provide both normal and test modes of operation.

Independent claims 8, 15, 22, 24, 26 and 28 all require that the same data paths are used in both the normal and test modes of operation. While appellants group the claims into two groups and argue only independent claims 8 and 15, it does not appear that these arguments are directed to independent claims 35, 41, 47 and 49, and the claims dependent thereon, which do not recite that the same data paths are used for both a normal and test mode of operation. While appellants grouped the appealed claims into two groups, choosing claims 8 and 15 as representative of these groups, we are not bound to appellants' selection of representative claims. We could have chosen claim independent 35, for example, which is broader, in some aspects, than independent claim 8. Claim 35 contains limitations which were not argued by appellants and, had the examiner presented a prima facie case of obviousness with regard to claim 35, for example, it would have been proper for us to sustain such a rejection in the face of appellants' lack of any argument with regard to this claim.

However, the examiner's position is that as to "claims 35-51, they fail to distinguish over rejected claims 8, 15-28, accordingly, they are rejected under the same

rationale..." (Paper No. 5-page 5). Clearly, whatever rationale was applied by the examiner against claims 8 and 15-28 is not appropriate for claims 35-51 since these claims (claim 35, for example) are completely different from claims 8 and 15. Thus, the examiner erroneously lumped claims 35-51 together with claims 8 and 15-28. Although claims 35-51 are nothing like claims 8 and 15, because the examiner grouped them all together, we have nothing from the examiner indicating any basis whatsoever for rejecting claims 35-51 over Bullinger.

Even though appellants present no arguments regarding the specifics, for example, of independent claim 35, we will not sustain the rejection of this claim, or any of claims 35-51, under 35 U.S.C. § 103 because the examiner has quite clearly failed to establish a prima facie, or any, case of obviousness with regard to the subject matter of these claims. This is not to say that there would be no rationale under which these claims may have been properly rejected in view of Bullinger. We do not know. We simply assert that, whatever case *might* have been made, the examiner has, quite clearly, not made it.

We have not sustained the rejection of claims 8-28 under 35 U.S.C. § 103 because we are not convinced that Bullinger suggests that the same data paths are used in both the normal and test modes of operation.

We have not sustained the rejection of claims 35-51 under 35 U.S.C. § 103 because, simply, the examiner has given us no reason for rejecting these claims.

Accordingly, the examiner's decision is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)
JERRY SMITH Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
MAHSHID D. SAADAT Administrative Patent Judge	)

eak/vsh

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